AMENDMENTS TO THE CLAIMS

Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method for managing power consumption in an electronic system, comprising:

providing a first processor of the system with a first task to perform;

providing a second processor of the system with a second task to perform, wherein performance of the second task will use a result of performance of the first task~~, and wherein the result of the performance of the first task is stored in a data store~~;

requesting an adjustment to an operating point of one of the first and second processors to better manage power consumption in the electronic system, based on a time between completion of the second task and its deadline; and

signaling of an interrupt to the first processor by the second processor upon completion of the second task, wherein the first and second processors perform their respective tasks according to triple buffered graphics processing ~~to indicate that the data store is available for use by the first processor~~.

2. (Previously Presented) The method of claim 1 wherein the requested adjustment is to decrease a frequency of a processor clock if said time indicates that the deadline was met.

3. (Previously Presented) The method of claim 1 wherein the requested adjustment is to increase a frequency of a processor clock if said time indicates that the deadline was not met.

4. (Original) The method of claim 1 wherein the first and second tasks relate to

describing and rendering images by the system, the method further comprising computing the deadlines of the first and second tasks based on a target frame rate for displaying images.

5. (Previously Presented) The method of claim 1 further comprising measuring an amount of time needed for the first processor to complete the first task and the amount of time needed for the second processor to complete the second task, wherein the requested adjustment is based on said measurements.

6. (Cancelled).

7. (Cancelled).

8. (Currently Amended) A method comprising:

providing a processor with a workload that has a real-time demand; and

setting a processor clock frequency requirement for the processor based on a deadline margin for the real-time demand, wherein the deadline margin is a measurement of a time between (i) completion by the processor of identifying one or more graphics surfaces in an image, and (ii) a start of rendering the one or more graphics surfaces and wherein the processor to signal an interrupt to a central processing unit (CPU) upon completion of the rendering the one or more graphics surfaces, wherein the processor and the CPU perform their respective tasks according to triple buffered graphics processing ~~to indicate that a data store is available for use by the CPU~~.

9. (Original) The method of claim 8 wherein the real-time demand is a target frame rate for displaying image frames.

10. (Cancelled).

11. (Previously Presented) The method of claim 9 wherein the margin is computed based on (i) an estimate of a time needed by the processor to identify one or more graphics surfaces in an image, (ii) an estimate of a time needed to render the one or more graphics surfaces, and

(iii) the target frame rate.

12. (Previously Presented) The method of claim 9 wherein the margin is a measurement of a time between (i) completion by the processor of rendering an image, and (ii) a start of displaying the image.

13. (Previously Presented) The method of claim 9 wherein the margin is computed based on (i) an estimate of a time needed by the processor to render an image, and (ii) the target frame rate.

14. (Currently Amended) A system comprising:

a central processing unit (CPU);

a graphics controller coupled to the CPU;

a monitor coupled to the graphics controller; and

memory containing instructions that, when executed by the CPU, (i) identify models of surfaces to be rendered in an image, wherein the image is to be rendered by the graphics controller and then displayed on the monitor in accordance with a target frame rate, and (ii) specify an operating point for one of the CPU and graphics controller, based on a deadline margin for the target frame rate, wherein the graphics controller to signal an interrupt to the CPU upon completion of at least one of rendering of the image and displaying of the image on the monitor, wherein the CPU and the graphics controller perform their respective tasks according to triple buffered graphics processing ~~to indicate that a data store is available for use by the CPU~~.

15. (Previously Presented) The system of claim 14 wherein the operating point is a value that represents one of (i) a clock frequency, (ii) an offset to the clock frequency, and (iii) a direction of increase or decrease in the clock frequency.

16. (Previously Presented) The system of claim 14 wherein the instructions, when executed by the CPU, specify the operating point of the graphics controller based on a time between when a rendering task is finished by the graphics controller and a deadline of the

task.

17. (Previously Presented) The system of claim 16 wherein the instructions, when executed by the CPU, specify the operating point of the CPU based on a time taken by the CPU to finish specifying mathematical models of graphics objects in an image and a time taken by the graphics controller to render the image.

18. (Previously Presented) The system of claim 14 wherein the instructions, when executed by the CPU, specify the operating points for the CPU and the graphics controller, based on values recorded in the system that represent an actual elapsed time needed to completely render an image by the graphics controller and an actual elapsed time needed to complete an identification of models of graphics objects in said image by the processor.

19. (Previously Presented) The system of claim 14 wherein the operating point is one of a high performance mode and a low performance mode for the CPU.

20. (Original) The system of claim 19 wherein in the high performance mode, the CPU operates at a higher clock frequency and at a higher supply voltage than in the low performance mode.

21. (Currently Amended) An article of manufacture comprising:

a computer-readable medium which has data that, when accessed by a processor, requests an operating point requirement for a target processor to (i) reduce power consumption by the target processor while the target processor performs a workload and (ii) meet a plurality of completion deadlines for a plurality of tasks in the workload, wherein the operating point requirement is based on an elapsed time between completion of a task and its deadline, and wherein the target processor to signal an interrupt to the processor upon completion of at least one of the plurality of tasks, wherein the processor and the target processor perform their respective tasks according to triple buffered graphics processing ~~to indicate that a data store is available for use by the processor~~.

22. (Previously Presented) The article of manufacture of claim 21 wherein the data is to define the operating point requirement as a decrease in a frequency of an operating clock for the processor.

23. (Original) The article of manufacture of claim 21 wherein the data is part of a computer operating system program.

24. (Original) The article of manufacture of claim 21 wherein the data is part of a computer system driver program.